

M. KOBAYASHI LAB.

Nanoscale Semiconductor Device for Computing



Department of Informatics and Electronics

Integrated Nanoelectronics

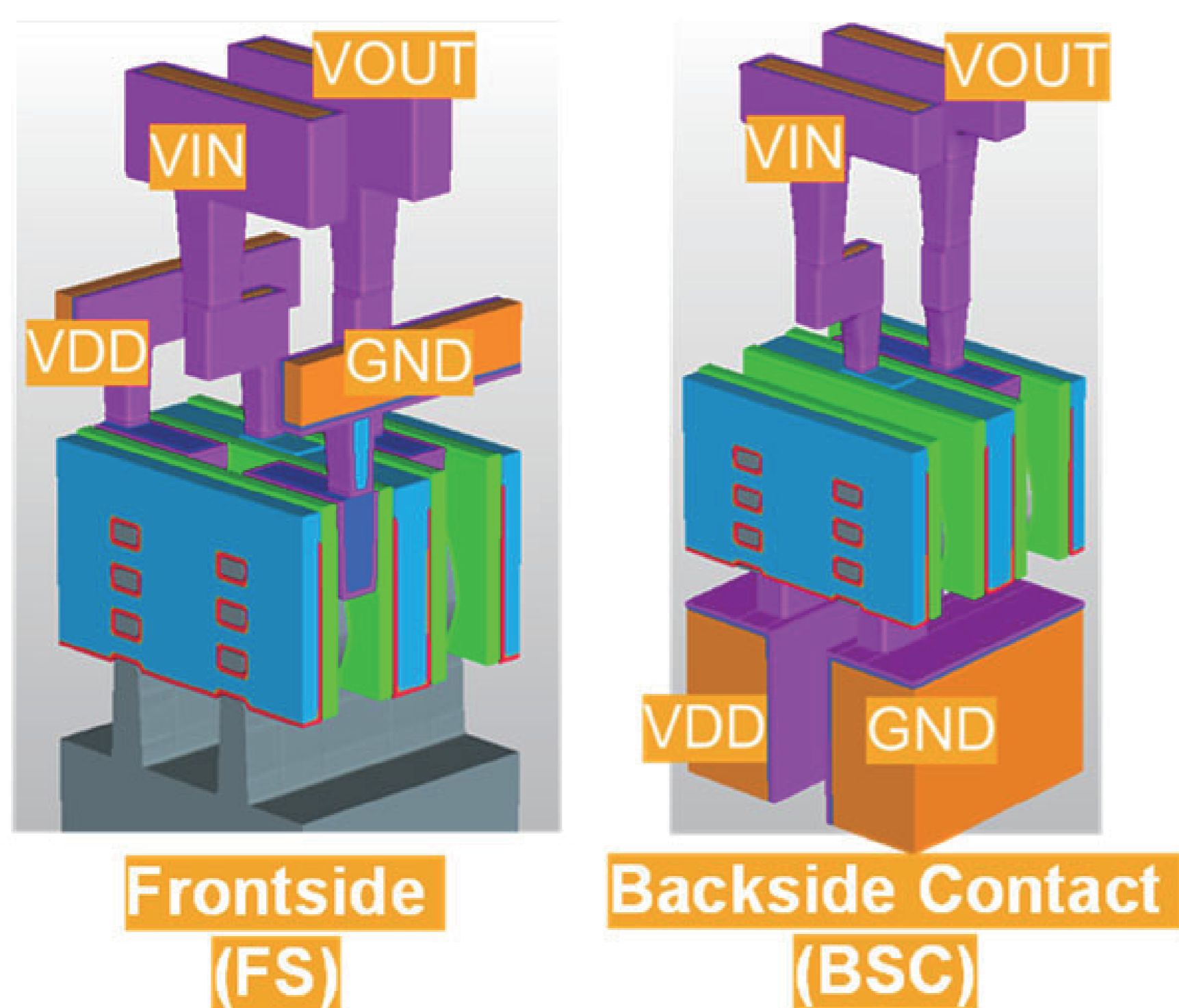
Department of Electrical Engineering and Information Systems, Graduate school of Engineering

<https://nano-lsi.iis.u-tokyo.ac.jp/en/home/>

Semiconductor Device Technologies for Computing

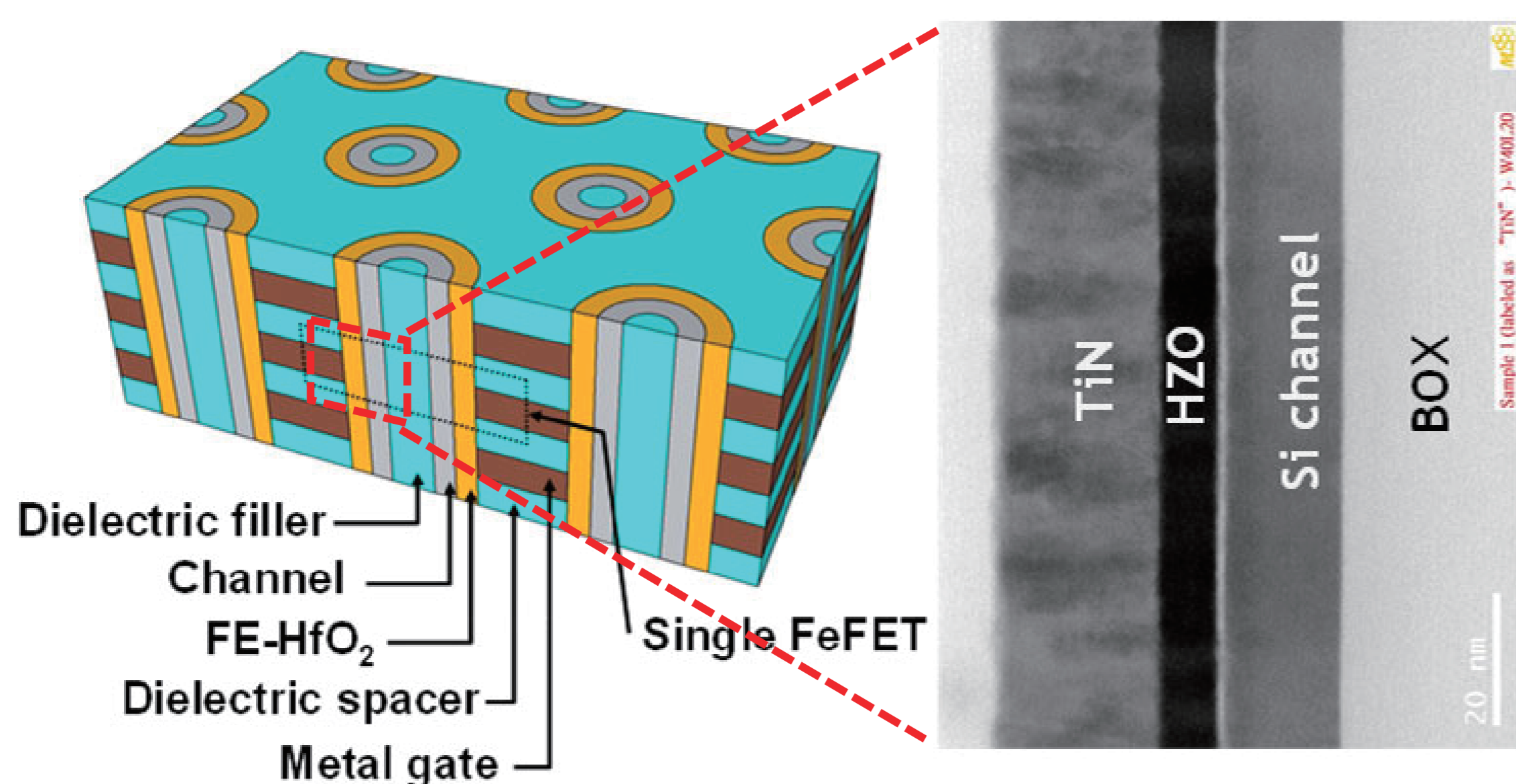
The advancement of AI technologies have been realized by semiconductor device technologies for computing. Further high-density, high-performance, and low-power semiconductor device technologies will be demanded. In our laboratory, next generation semiconductor devices are studied. In particular, we focus on semiconductor transistor scaling, high-density memory devices, and 3D integration.

Design-Technology Co-Optimization (DTCO) in Advanced Logic Semiconductor

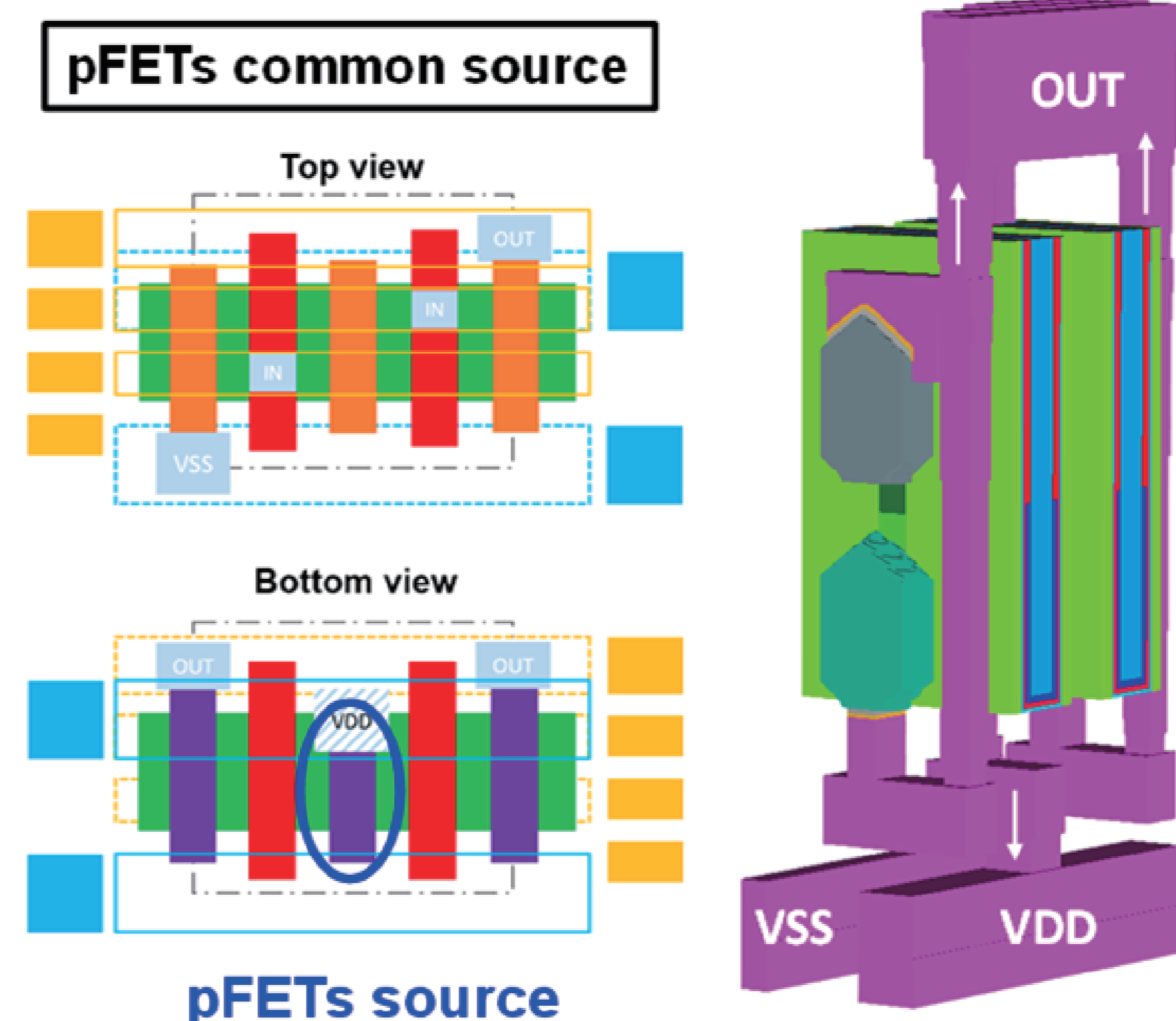


Power-performance optimization by back-side power delivery network (BSPDN)

High-density Memory Devices

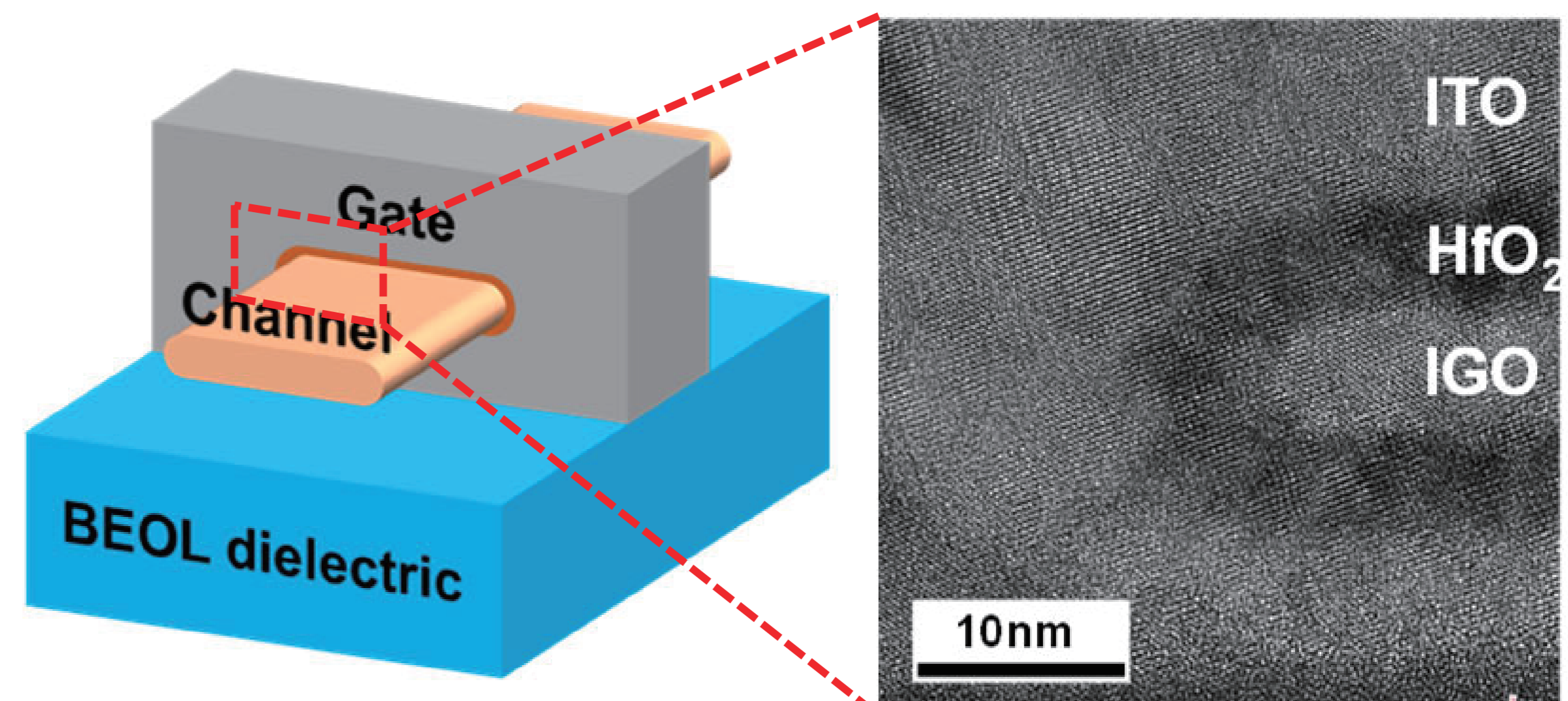


High-density, high-performance, and low-power HfO₂-based ferroelectric transistor memory



Standard cell design for CFET technology

3D Integration Technology



3D-stackable Gate-All-Around oxide semiconductor transistor