SAKURAI LAB.

[High Speed Three-dimensional VLSI System with Low-Power Consumption]

Department of Informatics and Electronics

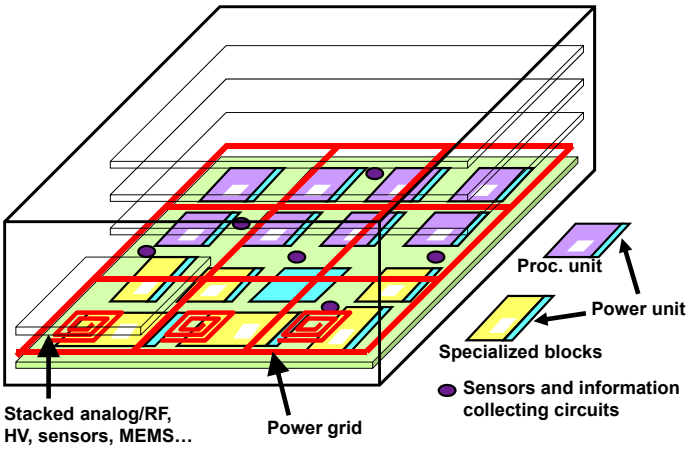
http://lowpower.iis.u-tokyo.ac.jp

Integrated Circuits and Systems Design

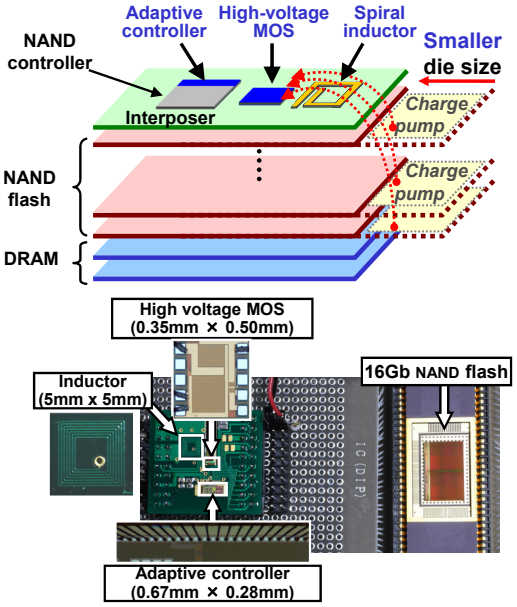
Department of Electrical Engineering and Information Systems

High Speed Three-dimensional VLSI System with Low-Power Consumption

It is very crucial for the last resort to suppress power consumption by reducing mutual communication energy with filling up the switch called transistor. Therefore, a three-dimensional layer system or eco-chip, that raises the density of the transistor by layering the chips three-dimensionally, has been considered. The laboratory has proven wireless connection between three-dimensional layer chips, which attracted great attention. Recently, research on transmitting electric supply between chips wirelessly has been in progress. The laboratory is leading the world in the research on an applicable chip which searches for a low-power operation point while observing own physical condition.

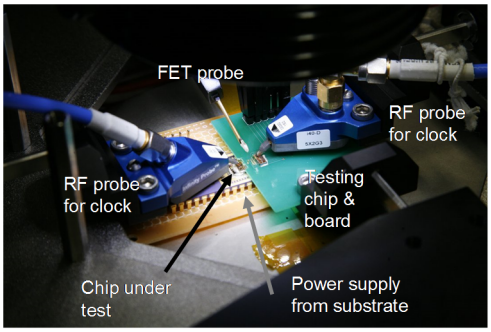


A smart 3D VLSI system observing own physical condition and carrying self-healthcare



Power supply system for 3D Solid-State Drive

Large-area electronics that consists of silicon LSI and various devices



Measuring the test chip designed in the laboratory