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HIRAMOTO LAB

[Silicon Nanotechnology and VLSI Devices]

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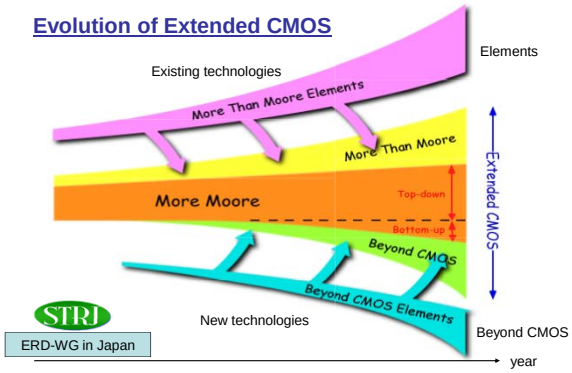
Integrated Device Engineering

Department of Electrical Engineering and Information Systems

Background and Targets

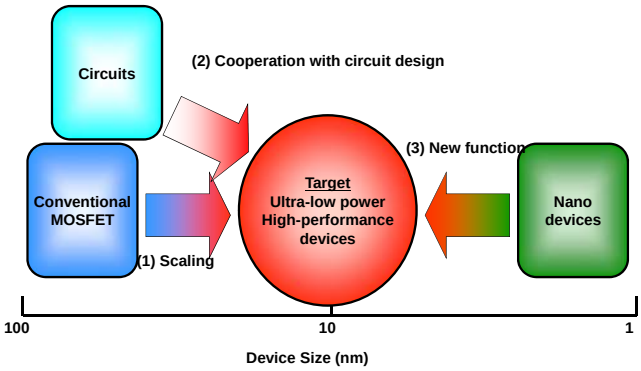
CMOS Technology in Future

Our vision for future CMOS technology is shown below. So-called Beyond CMOS devices will be merged into CMOS platform to form ultimate "Extended CMOS".



Approaches to the Targets

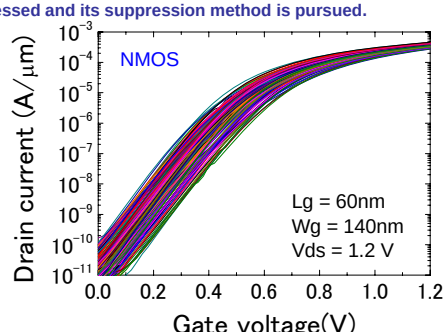
We adopt three approaches to the targeted ultra-fast low-power ultimate CMOS devices.



Main Achievements

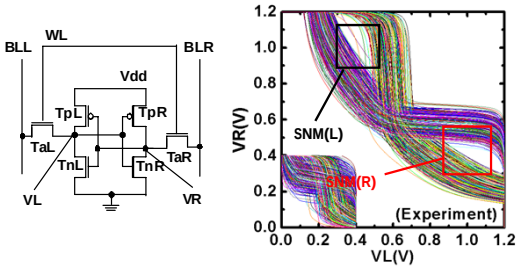
Characteristics Variability in Scaled CMOS

Transistor variability, one of the most serious problem in VLSI, is addressed and its suppression method is pursued.



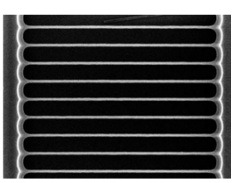
SRAM Instability

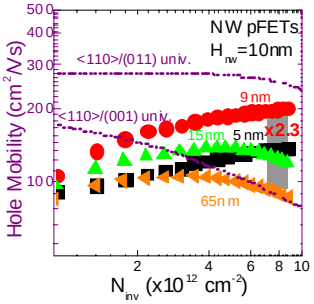
SRAM, a memory for logic circuits, is easily affected by variability. In our lab, the butterfly curves of SRAM cells can be directly measured.



Silicon Nanowire Transistor

Silicon nanowire transistor is promising for future VLSI. Mobility enhancement in silicon nanowire transistors has been experimentally demonstrated for the first time.





Silicon Single-Electron Transistor

Single-electron transistor is an ultimate electron device. We observed record high peak-to-valley ratio in a silicon single-electron transistor at room temperature.