HIRAMOTO-KOBAYASHI LAB.

[Silicon-Based Integrated Nano-Devices]

Department of Informatics and Electronics

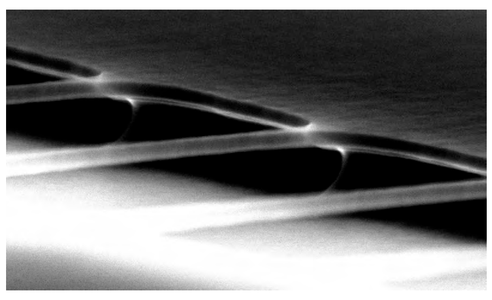
Integrated Device Engineering

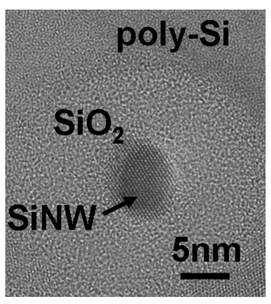
Department of Electrical Engineering and Information

http://vlsi.iis.u-tokyo.ac.jp/

Towards VLSIs integrating everything

Very large scale integration (VLSI) is the basis of contemporary advanced IT society. Hiramoto/Kobayashi Lab. aims at solving worldwide problems by the technological innovation of future integrated nanoelectronics from the device side. Prof. M. Kobayashi, formerly a researcher in IBM Watson Research, joined the lab in 2014. Based on the vision in Fig. A, we are pursuing the extreme form of integrated nanodevices.





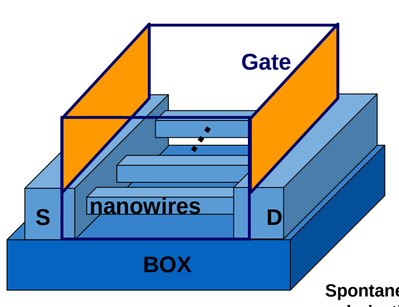
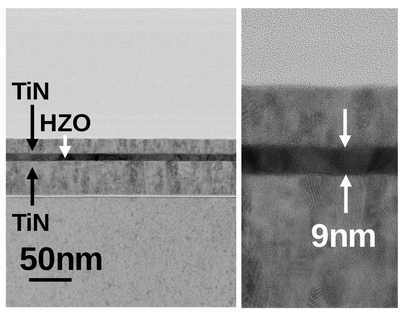


Fig. 1. Silicon nanowire transistors were fabricated and the quantum effects were evaluated.



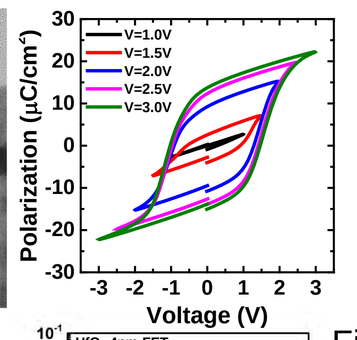
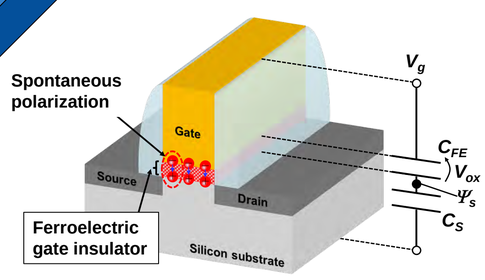


Fig. 3. (Top) Sub-10nm ferroelectric nano film is an enabler for ultralow power logic and memory technology with CMOS compatibility.



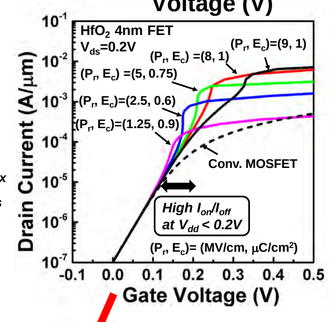
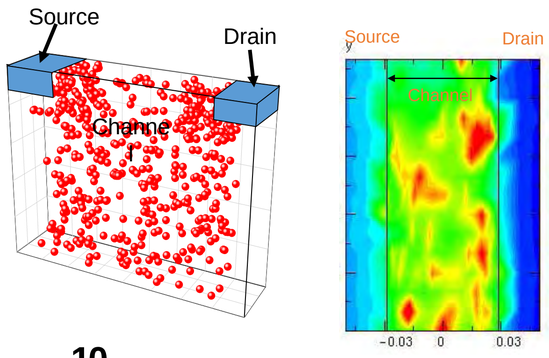


Fig. 3 (Bottom) Negative capacitance FET (NCFET) overcomes the theoretical limit of sub-threshold slope and achieve high I_{on}/I_{off}



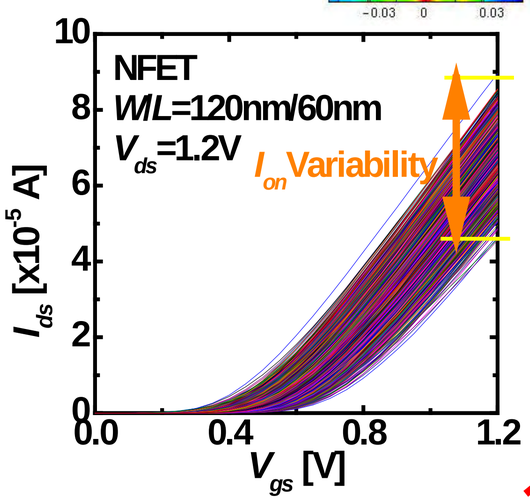
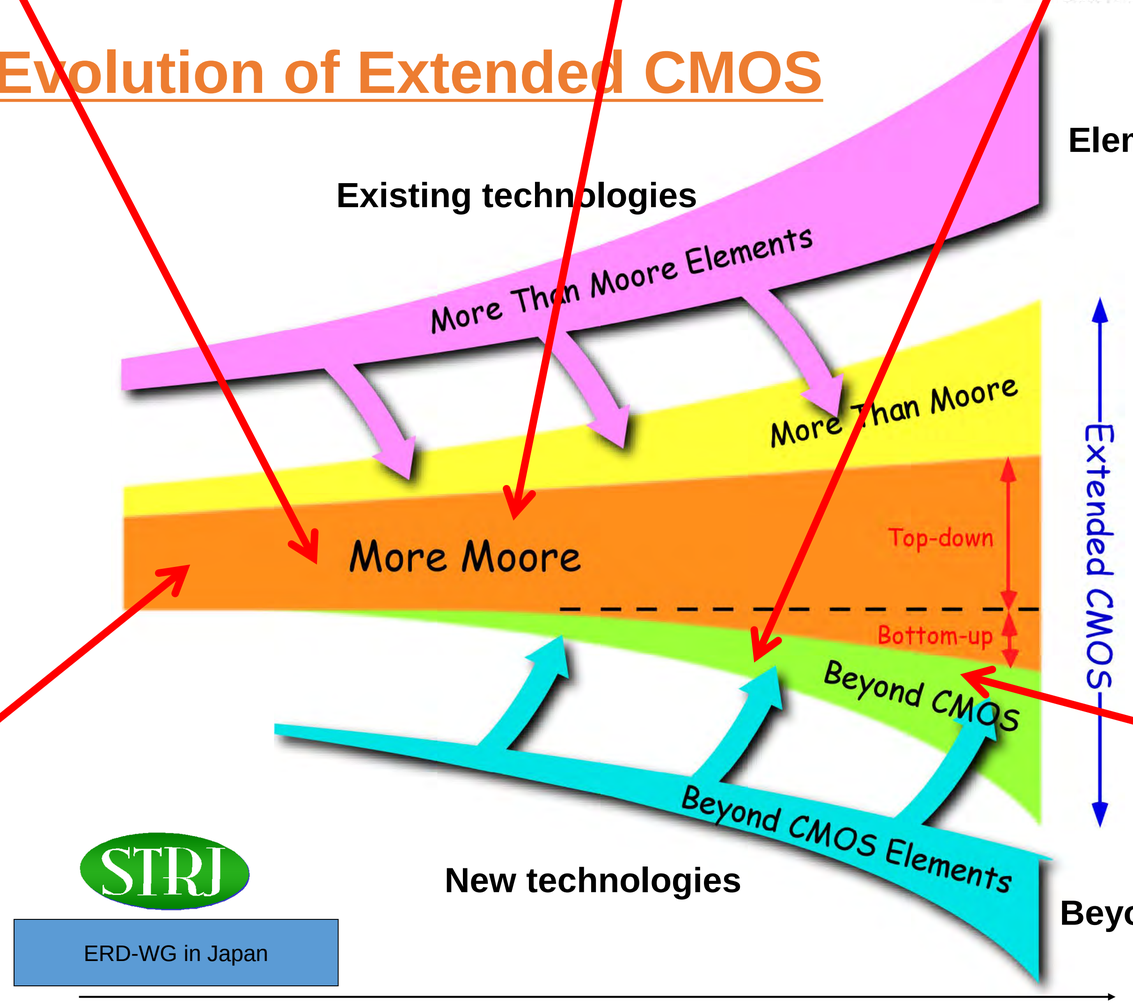
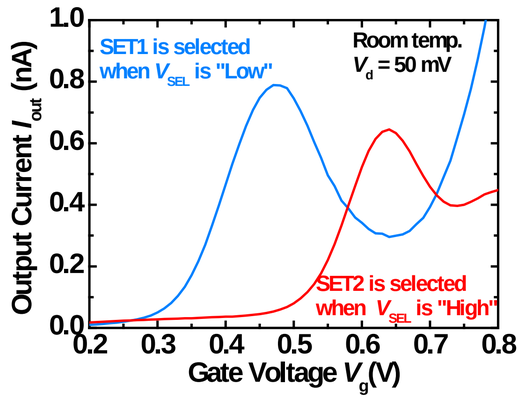


Fig. 2. Random variability of transistor characteristics is analyzed and its suppression method is proposed.





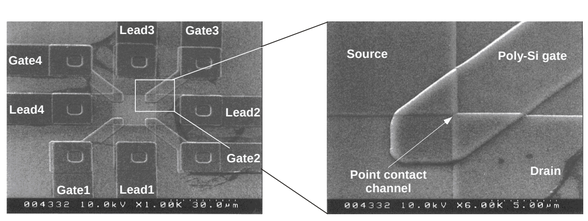


Fig. 4. Single electron transistor, one of Beyond CMOS devices, operating at room temperature is integrated into CMOS.

Fig. A. A vision map of the integrated nanoelectronics, drawn by Prof. Hiramoto in Semiconductor Technology Roadmap Committee of Japan (STRJ). A new field of “Extended CMOS” will be created by integrating “Beyond CMOS” and “More Than Moore” into CMOS base technology. This map is found in International Technology Roadmap for Semiconductor (ITRS).