

HIRAMOTO-KOBAYASHI LAB.

[Silicon-Based Integrated Nano-Devices]

Department of Informatics and Electronics

<http://vlsi.iis.u-tokyo.ac.jp/>

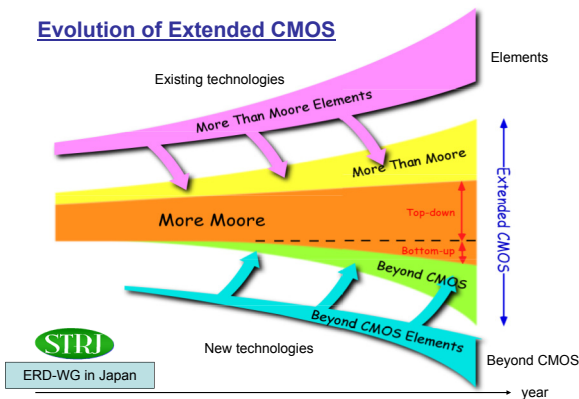
Integrated Device Engineering

Department of Electrical Engineering and Information Systems

Background and Targets

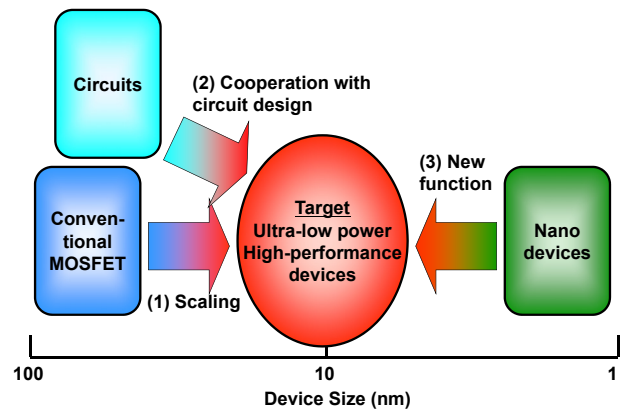
Future Trend of Integrated Electronics

Our vision is "Extended CMOS", where various "Beyond CMOS" devices are merged into the mainstream "More Moore" technology.



Target and Three Approaches

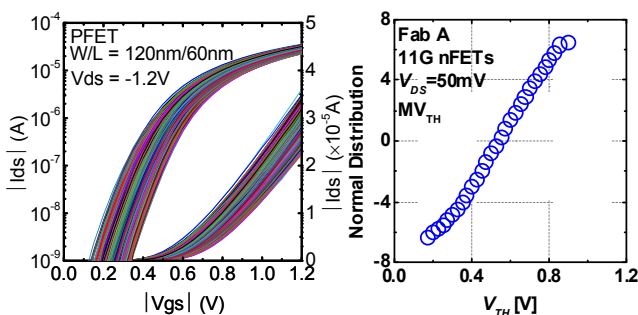
The target is ultra-low power integrated CMOS devices in the future. We are making progress by three different approaches.



Achievements

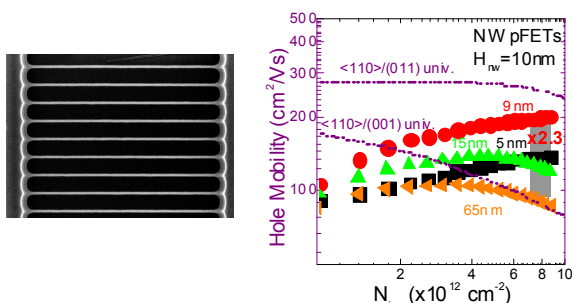
Variability in Scaled Transistors

The variability is one of the most severe problems for further scaling and lowering supply voltage. The variability of as many as 10G transistors is successfully measured and the origins of variability are clarified.



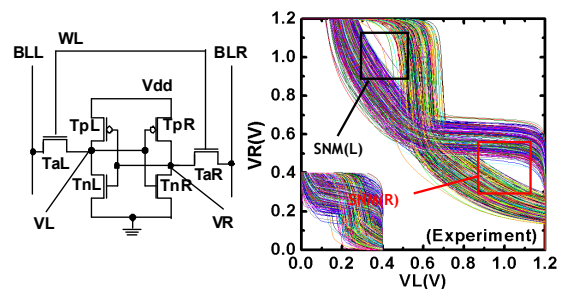
Silicon Nanowire Transistor

Silicon nanowire transistor is one of the most promising device structures. Higher hole mobility than the universal mobility is observed in silicon nanowire transistors for the first time.



Self-Improvement of SRAM Stability

The stability of SRAM is degraded by transistor variability. A novel post-fabrication self-improvement technique of SRAM cells has been proposed and demonstrated.



Silicon Single-Electron Transistor

Single-electron transistor (SET) is one of the ultimate electron devices. SETs are fabricated aiming at future integration into CMOS VLSI. The world largest Coulomb oscillations have been observed. Multiple SETs are integrated and controlled by CMOS circuits successfully.

